Generating *All* 2-Transistor Circuits Leads to New Wide-Band CMOS LNAs

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Abstract

This paper presents a methodology that systematically generates wide-band CMOS Low Noise Amplifiers (LNAs), assuming that MOSFETs are exploited as a Voltage Controlled Current Source (VCCS). Using graph theory, ALL 2-VCCS LNAs are generated, and subsequently implemented using 2 NMOS transistors. Next to well-known circuits, two new wide-band LNAs are found. The most promising has been realized using an industrial 0.35mm CMOS process. Measurements show a 900 MHz bandwidth, $VSWR_{IN}$<1.6, variable forward gain from 6 to 11dB and reverse isolation better than 30dB. At maximum gain, IIP2 is +15dBm and IIP3 is +1dBm, while NF is better than 4.5dB. The LNA drains only 1.5mA at 3.3V supply and the die area is 0.06mm^2.

1. Introduction

As the telecom revolution progresses, RF designers continue to be challenged by increased performance demands over the transceiver's analog building blocks in terms of higher speed, wider dynamic range and lower power consumption. The design of a wide-band low-noise amplifier (LNA) with a mainstream digital CMOS is an example. Wide-band LNAs find several applications in cable modems, cable TV systems, base-stations, high-data rates communication systems and multi-band radio receivers. Nevertheless, we find in literature only a few wide-band CMOS LNA circuit alternatives [1,2]. New circuit topologies are normally found by designers based on creativity, intuition and experience. In contrast, we propose a *systematic* methodology that generates *ALL* 2-transistor wide-band CMOS LNAs. It is our believe that in this way we can find new useful circuits since: (a) Known LNAs are often simple circuits with only few transistors in the signal path (e.g. common-gate stage) (b) Two-transistor structures can be used as basic building blocks to make more complex LNA circuits [1,2]. Using our systematic generation approach [3] it will be shown that next to well-known LNA circuits such as the common-gate and the shunt-feedback common source stages, *two* new wide-band LNA circuits are found.

The paper is organized as follows. Section 2 deals with the systematic generation of 2-transistor CMOS wide-band LNAs. Section 3 gives a simplified analysis of a selected LNA. Section 4 shows the LNA realization and experimental results. Conclusions are in section 5.

2. Systematic generation

As mentioned before, we want to generate ALL wideband LNA circuits, which are possible with two transistors. Since a MOSFET has basically 3 terminals, there are already a lot of possible combinations, even if we limit ourselves to the case of a two-ports connected between signal source and load impedance. In order to streamline the searching process, a systematic method is used [3]. First a generalization step is made: a MOS transistor is considered as a Voltage Controlled Current Source [4] (VCCS, see fig. 1).

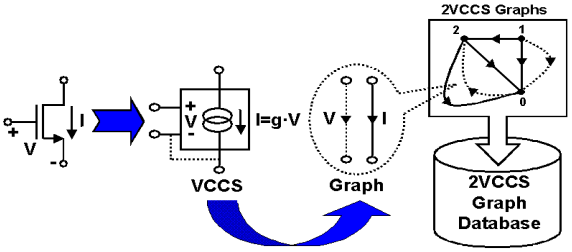
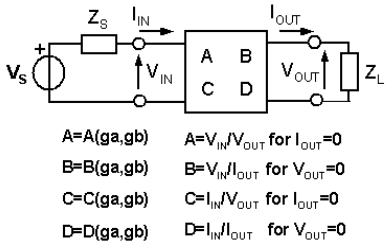


Fig. 1: NMOS modeled as VCCS and its graph representation. Using graph theory, ALL the topologies with 2 VCCSs have been generated systematically [3].

By doing so automatically NMOS and PMOS transistors are covered, and even combinations of MOSFETs and resistors acting as a VCCS. Also simple resistors are included, as they can be considered as a VCCS with additional wires, implementing R=1/g. The next step is to represent the VCCS as a linear graph (see fig. 1). Graph theory can now be applied to generate ALL possible 2-VCCS graphs, without finding the same one twice. This leads to hundreds of graphs, most of which represent useless two-port circuits (e.g. no solution or no signal transfer). It can be shown that useful two-ports should have at least one non-zero transmission parameter [5]. For circuit with two VCCSs the transmission parameters are determined by the transconductances ga and gb of the two VCCSs:



Using a symbolic analysis program all possible 2-VCCS circuits have been analyzed, yielding 145 useful 2-VCCS circuits. These implement a variety of "transactances" (V-V, V-I, I-I, I-V) with low, high and accurately defined port impedances. Note that each of these graphs can be implemented in several ways, since a VCCS can be implemented by a resistor, NMOST, PMOST, or combinations of them. More details can be found in [3]. Our LNA generation problem can now be redefined as finding 2-VCCS graphs, which can act as a wide-band LNA. To do so, we have developed a 3-step methodology (see Fig. 2):

1. The small-signal behavior of a wide-band LNA is defined through proper functional requirements on forward gain A_{VF}, input impedance Z_{IN}, bandwidth, and stability (see Tab.1). Using two-port equations eqn. (1), the requirements in Tab.1 are translated into constraints for the {A, B, C, D} parameters such as: (a) Useful combinations of non-zero {A, B, C, D} parameters. For instance, the combination {A,B,C,D}={0,B,0,D}is not suitable for our purpose as the forward gain $A_{VF}=1/(B\cdot SC_L)$ is not wide band. (b) {A, B, C, D} parameter values. This has been done assuming a resistive source $Z_S=R_S$ (e.g. cable characteristic impedance) and a capacitive load $Z_L=1/SC_L$ (e.g. mixer input gate capacitance).

Table 1: Wide-band LNA functional requirements.

Stability	Z_{IN}	$\lvert A_{VF}\rvert$	Bandwidth
Unconditional	Matching	>1	Wide

$$Z_{IN}=\frac{Z_L A+B}{Z_L C+D} \quad Z_{OUT}=\frac{Z_S D+B}{Z_S C+A}$$
$$A_{VF}=\frac{Z_L}{Z_L A+B} \quad A_{VR}=\frac{AD-BC}{D+\frac{B}{Z_S}} \quad (1)$$

2. The 2-VCCS graphs database is explored for circuits that do meet the previous requirements. The latter are ALL the 2-VCCS wide-band LNAs.
3. Transistor level implementations are obtained replacing VCCSs with NMOS transistors (because they are faster than PMOS) or, if possible, with simple resistors. Circuit arrangements that re-use DC bias current have been preferred. Doing so, the number of bias sources is minimized possibly lowering DC power and limiting the performance degradation due to bias circuitry (e.g.: noise).

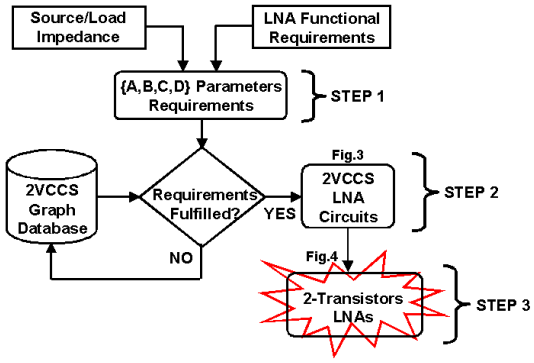


Figure 2.: Flow-chart of the developed systematic generation of ALL 2-transistor wide-band LNAs.

Fig.3 shows the 4 wide-band 2-VCCS LNA circuits, which are the output of step 2 of the generation methodology. In Fig.4 the selected transistor level implementations are shown (signal path only).

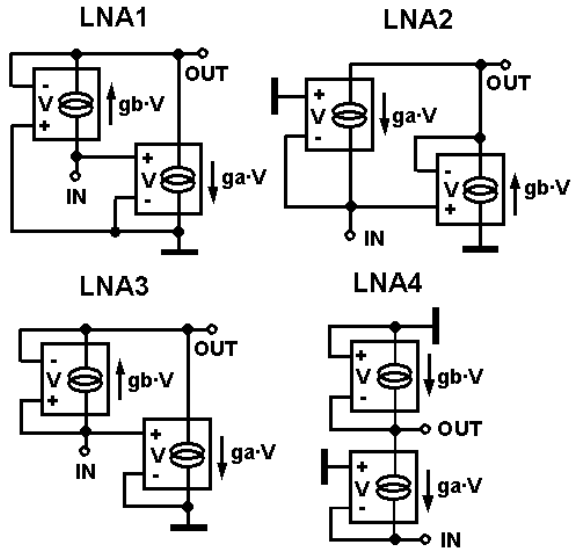


Figure 3: Generated 2VCCS LNA circuits.

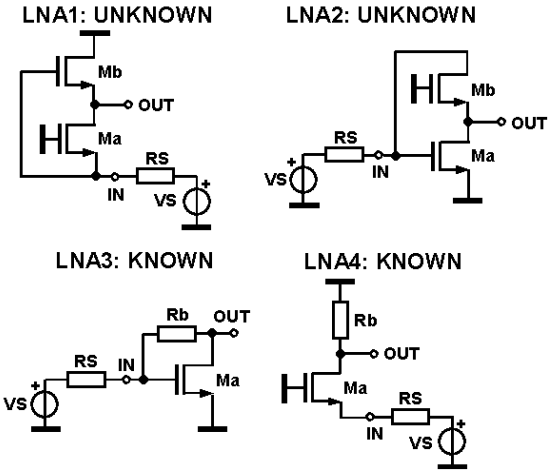


Figure 4: Generated 2-transistor wide-band NMOS LNA circuits (signal path only).

Next to well-known LNA circuits such as the common gate (LNA4) and the shunt feedback common source (LNA3) stages, two other wide-band CMOS LNA circuits (LNA1 and LNA2) are found. The latter, as far we know, are new wide-band CMOS LNA circuits. In the next section we will focus on the most promising of these 2 circuits: LNA1. Analyzing these two circuits, LNA1 was recognized to be more attractive than LNA2 as: (a) In contrast to LNA2, LNA1 does not relay on feedback. Thus, here stability is not an issue. (b) LNA2 has lower reverse isolation. This is because any voltage variation at the output node generates a current that directly flows to the input node.

3. LNA1 simplified analysis

We now analyze the small signal and noise properties of LNA1. To gain useful insight about its operation, we analyze LNA1 modeling the MOS transistor as a VCCS. This is because: (a)Node impedances exhibit a 1/g-type dependence. (b)For a MOS, $g_m >> g_d$ typically holds.

3.1 Small signal parameters

In Table 2 the main small-signal parameters are shown. The common-gate transistor Ma provides the required wide-band input impedance $Z_{IN}=1/g_a$. The voltage gain $A_{VF}=A_{VF,1}+A_{VF,2}$ is the result of the superposition of gain contributions of two stages: a common gate Ma-Mb with $A_{VF,1}=g_a/g_b$ and a source follower Mb with $A_{VF,2}=1$ (neglecting body effect). Thus, LNA1 can easily provide a gain higher than 1. Furthermore, by varying g_b, variable gain can be implemented. In LNA2 variable gain is easily hindered by stability problems. As LNA1 basically consists of two feed forward sub stages, stability is guaranteed.

Table 2: Small-signal parameters.

$1/Z_{IN}$	$1/Z_{OUT}$	$A_{VF}=V_{OUT}/V_{IN}$	$A_{VR}=V_{IN}/V_{OUT}$
g_a	g_b	$1+g_a/g_b$	0

3.2 Noise factor

MOS channel thermal noise is linked to device small-signal transconductance g_m as:

$$\frac{\overline{di_d^2}}{df} \equiv 4kT \cdot NEF \cdot g_m \qquad (2)$$

where NEF is the transistor noise excess factor and NEF>1 holds for a modern CMOS process. Noise analysis shows that the minimum noise factor NF of the LNA is similar to that of a common-gate stage:

$$NF \approx 1 + NEF \qquad (3)$$

4. LNA1 realization and measurements

Fig.5 shows the schematic of a 900MHz variable gain wide-band CMOS LNA based on LNA1 topology. This LNA is designed to match a 75Ω source and must drive an on-chip capacitive load C_L (in the test chip a pad capacitance equal to 0.28pF is used as load). Variable gain from 6 to 12dB is obtained changing the width of transistor Mb1 in 4 discrete steps (through Mb2 and Mb3). This is done placing two PMOS switches MD1 and MD2 in series to the drains of Mb2 and Mb3. Doing so, switches do not degrade NF and bandwidth being out of the signal path. The gates of transistor Mb1-Mb2-Mb3 are 'ac' coupled to the RF input by a simple C-R (CB1-RB1) high-pass filter with a 1 MHz +3dB corner frequency. CB1 is large enough to limit the NF degradation (at the low side of the frequency band) due to RB1. For biasing purpose, transistor M4-Ma and resistors RB2-RB3 perform a current mirroring function. For "dc" the gate of Ma is connected to that of M4 (M3= high resistance), while for 'ac' capacitance CB2 shunts the gate of Ma to VSS.

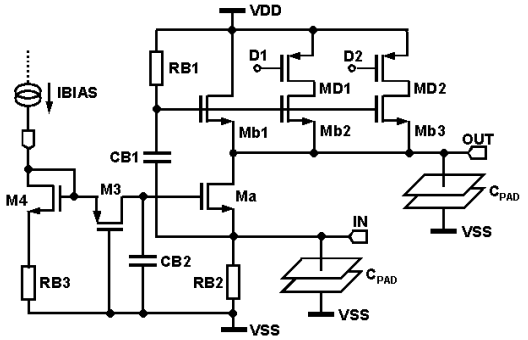


Figure 5: Schematic of the wide-band CMOS LNA based on the LNA1 topology concept.

RB2 can increase the noise figure. A value of 750Ω is used to limit this NF degradation, still keeping enough voltage headroom for the circuit. In order to reduce chip area capacitances CB1 and CB2 have been implemented using MOS transistors. Fig.6 shows the photo of the chip realization using an industrial 0.35μm CMOS process.

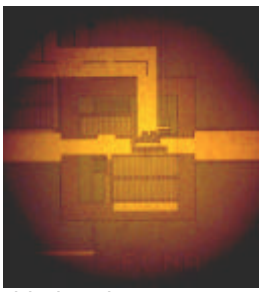


Figure 6: Wide-band CMOS LNA chip photo.

Forward gain A_{VF}, reverse gain A_{VR} and input $VSWR_{IN}$ has been obtained (see fig.7) from on-wafer S-parameters measurements. Forward gain A_{VF} varies from 6.2 to 11dB and the worst case –3dB bandwidth is above 900MHz. Reverse gain A_{VR} is better than –30dB. The increase of A_{VR} at high frequency is due to Mb, which introduces an input-output capacitive coupling. $VSWR_{IN}$ is less than 1.6. Fig.8 measured IIP2 and IIP3. IIP3 is +1dBm and IIP2 is +15dBm for max gain.

Table 3: Measurements at maximum gain

A_{VF}	11 dB
-3dB Bandwidth	900 MHz
$VSWR_{IN}$	< 1.6
A_{VR}	< -30dB
IIP2	15dBm
IIP3	1dBm
NF	< 4.5 dB
Supply voltage	3.3V
Supply current	1.5mA
Technology	0.35μm CMOS
Die arena	0.06mm^2

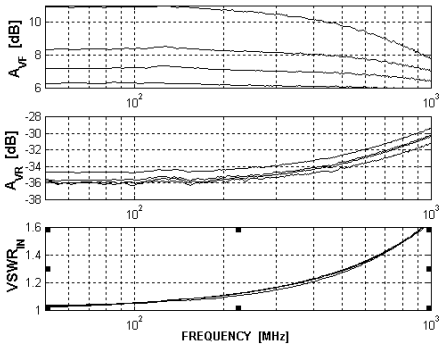


Figure 7: Measured A_{VF}, A_{VR} and $VSWR_{IN}$.

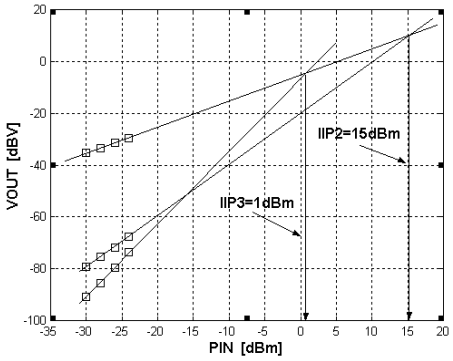


Figure8: Measured IIP2 and IIP3 for max (min) A_{VF}.

The Noise figure measurement requires special attention as the LNA is designed to drive a capacitive load (direct connection to the HP8970B noise figure meter is not possible since the 50Ω termination would shunt the LNA output impedance, so killing the voltage gain). To overcome this problem the required matching has been achieved using microwaves tuners. However, due to tuners limitations NF has been measured starting from 500MHz (see Fig.9). Clearly, for max gain a NF ranging from 4.2 to 4.5dB can be observed. This value is rather close to the one predicted by eqn. (4) as 1+NEF=2.5 (for this technology NEF=1.5 at low Vgs). A NF of about 4.5dB is required for instance in cable modem applications [6]. The LNA drains only 1.5mA at 3.3V supply and the die area is 0.06mm^2.

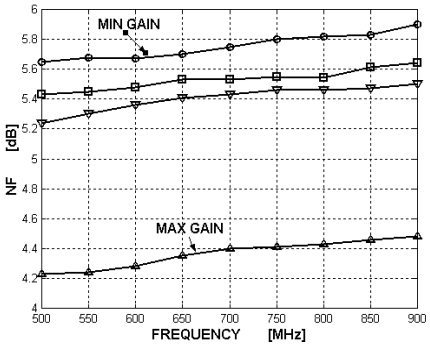


Figure 9: Measured NF for different A_{VF} settings.

5. Conclusions

A methodology generating systematically ALL 2-transistor wide-band LNAs has been presented, resulting in *two* new circuits. A variable gain wide-band LNA has been realized using an industrial 0.35μm CMOS process. The LNA has gain between 6 and 11dB and more than 900MHz bandwidth at only 1.5mA and 3.3V supply. Measurements for maximum gain are listed in table 3.

Acknowledgments

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6. References

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