"Chasing Time" or who is chasing what

The laboratory for IC-Design anno 2000

As time goes by....people start chasing other issues

Since May 1998 the laboratory of IC-design is chaired by prof. Bram Nauta. Until that time the group's research has been roughly for one half aiming on "low frequency" high efficiency Audio-systems and for the other half on "high frequency" circuits and systems in which we considered research on 100MHz filters as Chasing High Frequencies.
The group's research is now focusing on circuits and systems for modern telecommunications, in which much higher operating frequencies are at stake. The bulk of today's signal processing is digital, so telecommunication is mainly characterized by "Transferring bits from A to B", both by network and on-chip.
In most systems the received or transmitted signal is an amplitude, frequency or phase modulated carrier wave. Network cable capacity is nowadays being exploited to its upper limit by, amongst others, using multi-level digital signals. That is why part time prof. Ed van Tuijl shifted his attention from audio frequencies to modern modem techniques. In his (optional) course "Integrated Circuits and Systems for mixed signals" IC's for RF and cable modems get full attention. Of(f) course he is grimly chasing for students..... Indeed the bulk of the signal processing is digital, the interfacing to cables and antennas as well as to telephones, loudspeakers, cathode ray tubes and so on is to a very high extent an analog problem and it will remain so. So we are not only challenged to make high performance data-communication interfaces for both the receiver end and the transmitter end of the communication channel but we should do that preferably cheap, so it comes within easy reach of all users. A robust IC- technology guarantees a reliable product for a reasonable price and as money is time, we could better chase money as there is a lot of it going on in this branch.

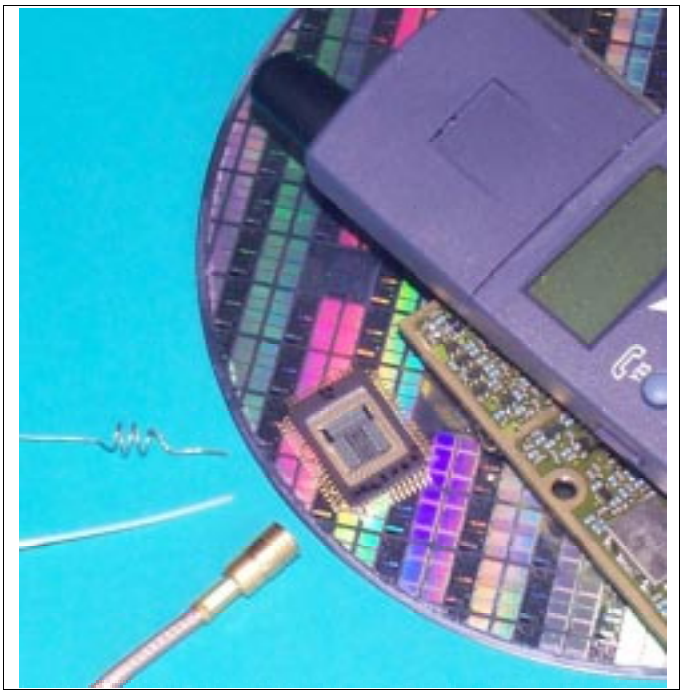

Figure 1 *The ever growing data stream is communicated via cable, antenna or fiber. Integrating the Transmitter and Receiver Interface to the communication channel on an Integrated Circuit (IC) is attractive for reasons of cost, size and power dissipation.*

For frequencies up to the lower GHz range (1 to 5 GHz) a standard digital CMOS technology can be successfully exploited. At higher frequencies (up to 50 or even 100 GHz) specialized RF technologies are used. In near future this might change with further downscaling of CMOS devices!

So our goal is to provide GHz circuits in the state of the art CMOS which is now a 0.18 µm technology.
In this frequency range the on-chip-dimensions are no longer negligible with respect to the signal's wavelength and micro wave techniques come in! We are very happy that in the past year with the help of industrial funding we successfully purchased a special chair on Microwave techniques, which since 1st of March 2000 is personalized by dr. ir. Joe Tauritz ! Prof. Tauritz is lecturing the course "Introduction on high frequency and micro wave techniques" with which he already chased several students from well known industrial plants in the near vicinity.

Why not surrender to digital instead of chasing Analog

The simple answer is, that the channel is not complete without the interfacing circuitry. The increasing number of digital operations that can be performed on an ever decreasing area of silicon would be useless if there is no valid A to D conversion, no antenna interface, no linear line drivers and so on. Moreover, pure two level digital signal processing is wasting a lot of channel capacity, while analog "multi-level signal processing" almost full channel capacity can be exploited.
One could say, that the analog art of designing is the yeast without which the digital bread is indigestible.
World wide network exploiters, be it in cable or wireless in "ether", are under constant pressure to carry increasingly more data per unit, are bound to squeeze existing cable (copper, fiber) networks' capacity to handle more bits per second. Now happily in the late forties Shannon chased for the maximum channel capacity C of a communication channel. He found that it is directly related to the bandwidth BW [Hz] and the Signal-to-Noise Ratio SNR. From this the "analog work space" can easily be read as:

- larger bandwidth, -so higher frequencies and higher speed and
- larger signal to noise ratio - so multi level signal processing and low noise.

Adjacent to exhausting existing copper cable nets, the net capacity is vastly extended by a huge amount of fibers, which can handle frequencies into the GHz range. Wall Street daily shows, that analog investments and laborious digging fiber cables into rocky ground are expected to pay off soon by "easily" selling channel capacity. We did anecdotically not chase for some World On Line shares.....

Now what do the analogs really chase for

Data transmission over cable comes with significant losses, especially at high frequencies. Therefore there is a need for (adaptable) line drivers and line receivers. Often data have to be stored, so writing an sensing data from memory has to be handled. These are typical analog design problems just as is high frequency clock distribution over a chip. Furthermore, almost all data communication systems divide the available bandwidth in sub-bands that are used by individual users. Thus receiver design generally involves channel selection, usually by means of a frequency synthesizer with a down converting mixer. So in addition to the earlier mentioned, the analog challenges can be summarized as:

- high frequency line drivers and line receivers

- sense and write amplifiers,
- AD and DA converters,
- switch able filters for channel selection,
- mixers and highly stable frequency synthesizers

Transcieving

To give a handhold, we look at the schematic of fig. 2, which gives a general impression of a data-communication process. As the receiving option is as good as the opposite of the transmitting option configuration, the set up of the configuration is quite symmetrical.
Now what are the specific analogue system parts in modern data transmission systems? If read from RF front end, following the arrows to back-end, it represents a receiver action from left to right, it represents a transmitter action from right to left. The receive and transmit action being almost each others mirrored operation, one generally indicates these systems as "transceivers".

Due to the amount of channels to be transceived, filter and amplifier have to be adapted regularly to the desired frequency band. This adaptation is being performed by the heart of the analogue part of the system: the frequency synthesizer. This (voltage) controlled oscillator is expected to select the right channel by using Time Division Multiple Access (TDMA) or Frequency Division Access (FDMA) systems , in the meanwhile co-adapting the filter operation as well as the AD clock reference and last but not least organizes the signal bits to come in or go out.

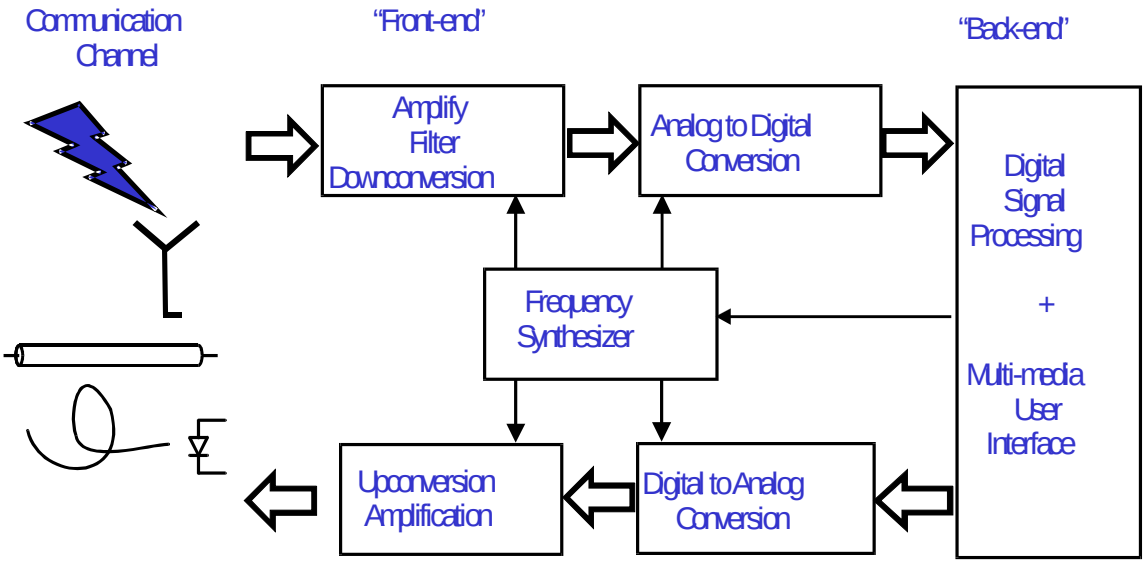

Figure 2: *Block schematic view of a transceiver. The data processing is done in the right hand digital signal processing core ("back end") .The data is coming in and going out via a "front-end" connected to a communication channel (air, cable or fiber interface). In the receive path the incoming signal is amplified and down-converted in frequency while unwanted signals are suppressed (filtering). A subsequent A/D converter converts to digital. At the transmit side a D/A converter produces an analog signal which is subsequently up-converted to the desired carrier frequency.*

Thus:

- the incoming signal is preferably directly bound "on chip". Integrated antenna, fiber-to chip technology, automatic adaptively to characteristic cable impedances are desirable properties of the transmitter.
- the amplifier gain has to be (automatically) controllable, its noise performance has to be excellent.
- the filter has to be designed on microwave compatibility, has to be very stable and automatically tunable.
- the frequency synthesizer (VCO) should have a linear control characteristic, has to be very stable (free of jitter), while
- the AD and DA converter are supposed to manage 8 to 12 bit linearity over a large range of clock frequencies.

so the world is challengely chasing for analog, but HOW do we meet (chasing) conditions ?

To compete in this fast evolving world, it is cost effective to have the analog circuits on the same chip as the digital ones. The most competing one is the most recent one: today's standard C-MOS which is characterized by a minimal device dimension (W,L) of 0.18µm; oxide thickness of 10 nm and transition frequency of 10ths of GHz.
Problems, which we prefer to declare as CHALLENGES, in implementing Transceivers in standard CMOS technology are manifold:

- Technology is scaling down, chasing for more functions per area, more products per unit time , in brief: chasing for more. To avoid device break down, lower voltages have to be applied. Therefore we have to design our circuits for low voltage (down to 1V)
- As an increasing amount of apparatus is battery fed, battery lifetime is more and more important. Designs have to be low power
- When integrated, digital switching bounces through the whole chip. To cope or better avoid digital interference, analogue designs have to be immunized, e.g. by smart balancing

Summarizing, CMOS-technology as a constraint does not only give us a lot of advantages. The summarized inconveniences however we like to embrace a equally many challenges, which we ARE GOING TO MEET in a scientific way, as indicates our mission statement:

Look for Fundamental Solutions for Practical Problems

In the present research approach, four items are our guideline:

1) Cooperation with industry (that is where ICs are being designed, that is were the practical problems originate from)
2) Thorough understanding of problem, we try to find its roots and subsequently try to solve it at its very roots or find reliable workarounds (fundamental solutions)
3) Look for architectural solutions (system level)
4) Explore/push limits of analog performance (device/circuit level)

now WHO do meet the challenges ?

In the past year we have happily been able to recruit a number of Ph D students, who are energetically tackling the most severe problems, which we will briefly discuss below.

No amplitude noise, please, Federico Bruccoleri

As Shannon's equation shows, channel capacity is benefited by as well large signal as a low noise level. Moreover the noise floor directly determines the maximum transfer distance for a radio link. Federico Bruccoleri is tackling the problem of the huge difference in signal level between full swing digital switching signals and RF oscillator signals (order of 1 V) on the one hand and weak RF antenna signals (order of μV) on the other. Due to the common substrate and IC package parasitics, the large signals can interfere with the weak antenna signal. The first block after the antenna is the analog amplifier. This amplifier has to contribute as little noise as possible, so main goal is to make it a "Low Noise Amplifier" (LNA). A systematic design approach is pursued by Federico, looking systematically for all possible circuit topologies with a given number of components. The result up to now is, that various new transistor configurations have come up. Simulation results render hopeful results and chip realizations are underway...

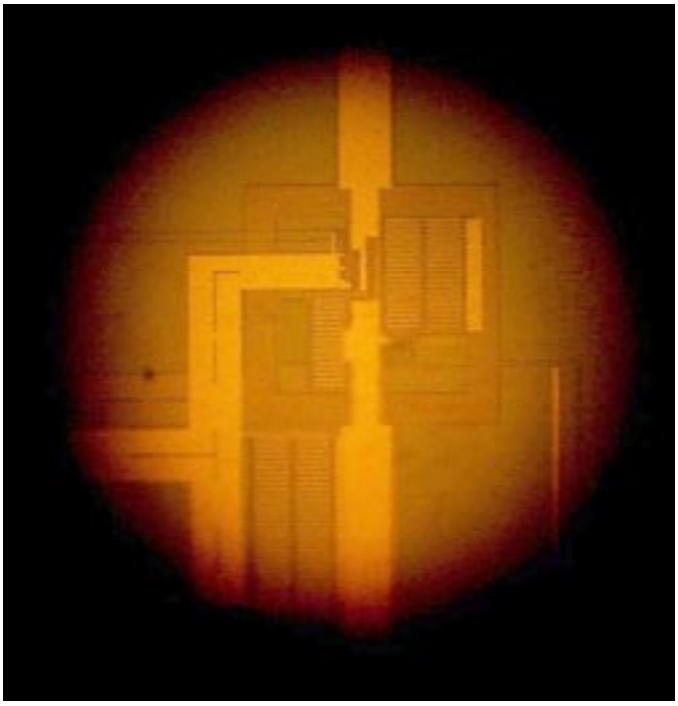

Figure 3 *Low noise requires low resistance requires broad leads requires large area, leading to large parasitic capacitance, which leads to a lot of thinking.....*

Chasing no phase noise

As amplitude noise gives rise to uncertainty of the signal's zero crossings, in oscillators this uncertainty leads to time or frequency uncertainty, so called "jitter". For frequency synthesizers in the GHz range this is lethal, because in the mixer the unwanted frequencies give rise to disturbed signal receipt. So Remco van de Beek is chasingly interrogating how to make VCO's with extreme stability and yet flexibility of the frequency synthesis. A stable frequency is a must !.

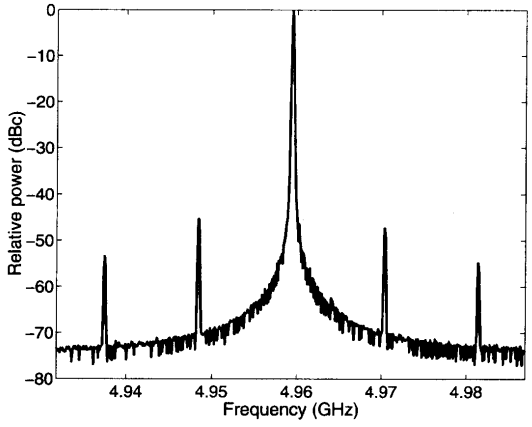

Figure 4 *There shouldn't be more than one peak...*

Noise free transistor operation

Analog electronic circuits exploit charge transfer in different ways. The MOS transistor's charge transfer is sometimes a severe bottle neck, because apart from "white" thermal noise, it suffers from so called "one-over-f-noise". Though this noise contribution is in the low frequency regions, in oscillators and mixers it is up-converted to Radio Frequencies (RF). In an earlier project Arnoud van der Wel in close cooperation with Sander Gierkink discovered, that 1/f noise gave a lower contribution if the transistor was periodically switched on and off during operation, mentioned as "switched bias operation". Up to now no reports on circuits exploiting this effect have been found and we cherish hope to be the first to explore it. Recently we showed that the effect of switching helps to reduce the phase noise in oscillators.
The aim of this project is to ***develop circuit techniques*** that exploit the physical effect of noise reduction by switched biasing. The project is financially supported by STW.

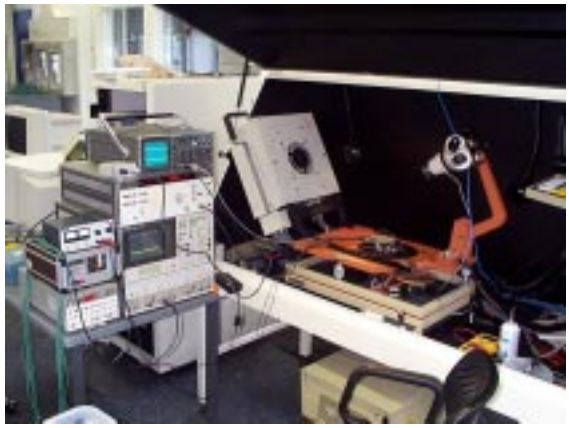

Figure 5. .... *measurements, which do not even add the slightest extra noise...*

Chasing small pixel low cost ADC

Applications are at the least as important as the circuits themselves. An interesting application comes from X-ray imaging, e.g. for chemical element detection as well as for medical applications. To enhance the contrast for a specific chemical element in X-ray imaging photons are counted. By measuring also their energy, a "color image" results, where different energy bands can be imaged separately. This could be applied e.g. to increase contrast between different tissues in medical engineering. A 4-6 bit ADC is then required, one ADC per pixel, directly mounted on the imaging array, so 10.000 ADC's in one chip! Between pixel and ADC there should be an "analog front end" to adapt the sensor signal to the ADC.
The challenges are then double: increased complexity and processing power of the pixel electronics, while at the same time aiming at low power and small pixel area ! David San Segundo Bello is in the spell of the design of this ADC. The research is carried out in close cooperation with the NIKHEF institute for high energy physics in Amsterdam.

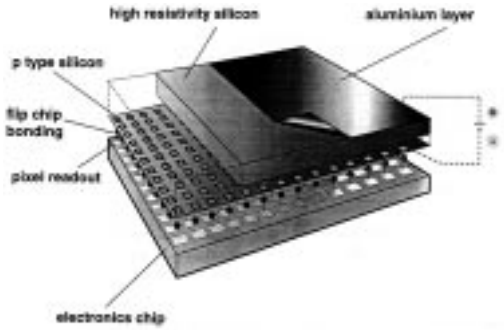

Figure 6 *Layers of a hybrid pixel detector, giving sight on the area where the adc is to be placed*

"Fiber" on chip

As the speed of microprocessors is increasing exponentially with time, data transport on chip must proceed with at least the same speed. For the future it is expected that these data-communication channels will become the speed-bottle-neck for the whole system. For this reason a research project in high-speed on-chip data communication is started. For short- and medium distance (centimeters up to hundreds of meters) the data communication channels are usually implemented as wired electrical connections. At high speeds however poor impedance matching results in distorted signals and significant Electro-Magnetic noise is generated. The problems with electrical wired communication channels could be circumvented by replacing the high-speed wired channels by high-speed optical communication channels. Due to the high bit rate and the big number of users the costs can be relatively low. For the medium and short distances as well as for a small number of users (fiber-to-the-home or fiber-to-the-desk) the optical receivers and transmitters should be really low cost. This project aims at increasing the speed and lowering the costs of the fully integrated optical receivers in standard CMOS technology. These receiver chips could have integrated light-sensors, which are cheap and do not have wire-speed limitations. Light propagates directly on the transistor's gate as it could propagate to the microprocessor. The result could then be a low-cost and high speed fully optical data communication system for distances ranging from chip-to-chip (cm range) up to LANs (up to hundreds of meters). Sasa Radovanovic is dedicating his time and energy in chasing for fiber on chip possibilities.

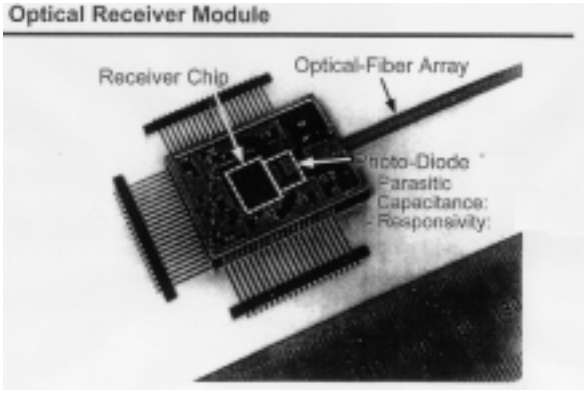

Figure 7 *Fiber to chip to (pur)chase speed....*

Chasing no voltage ADC

Svetoslav Gueorguiev is fully chased by the idea that high speed low voltage Analog to Digital converters are to be the indispensable building blocks in many systems. It's often a limiting factor in the overall performance .There are many strong trade-offs involved in the design of such a converter, e.g. speed v/s accuracy, noise v/s power dissipation and so on. The advance of the modern sub-micron CMOS processes with their reduced supply voltages makes its design even more challenging and requires innovative solutions.

This completes the Ph.D. projects and now students can drop by, have a drink and sign on for an interesting and particularly challenging assignment !!

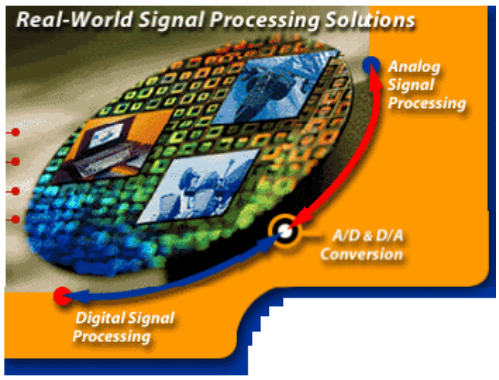

Figure 8 *Secret developments on ADC for RF applications, to be continued*